2011 International Workshop on ADC Modelling, Testing and Data Converter Analysis and Design and IEEE 2011 ADC Forum
June 30 - July 1, 2011. Orvieto, Italy.

High-Efficiency Cascade ΣΔ ADCs for Software-Defined-Radio Mobile Systems

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Abstract- This paper discusses a number of techniques to implement efficient cascade ΣΔ modulators intended for low-voltage, wideband, multi-mode applications. Several architectural strategies – such as loop-filter order reconfiguration and concurrency – are embedded in SMASH topologies with unity signal transfer function and resonation in order to improve the performance, while keeping high robustness against circuit errors. The proposed ΣΔ architectures – properly combined with circuit-level reconfiguration and biasing adaptation techniques – constitute a suited solution to implement analog-to-digital converters in future software-defined-radio mobile terminals.

I. Introduction

The road to future Software-Defined-Radio (SDR) mobile terminals will require System-on-Chip (SoC) transceiver solutions, implemented using mainstream nanometer CMOS processes as the base technology and embedding digitally-assisted adaptive analog front-ends. One of the key elements of these systems is the Analog-to-Digital Converter (ADC), since increasingly more signal processing is moving from the analog to the digital side, taking advantage thus, of programmability, firmware upgrading and technology down-scaling [1].
State-of-the-art multi-standard, multi-mode ADCs have been mainly implemented using Sigma-Delta Modulators (ΣΔMs) [2]. Based on the combination of oversampling and quantization noise shaping, ΣΔ ADCs achieve a high degree of flexibility as well as robustness with respect to physical-level effects. However, the increasing demand for high data rates forces using low values of the oversampling rates, what has prompted the exploration of more efficient techniques to implement high-order ΣΔM loop filters. Examples of these techniques include the use of Unity Signal Transfer Function (USTF) to relax amplifier requirements [3]; loop-filter resonation to optimally distribute the zeroes of the Noise Transfer Function (NTF), and the so-called Sturdy MASH (SMASH) topologies, that eliminate the need of digital filtering in the error cancellation logic [4].
In spite of the mentioned advantages, the practical implementation of the these strategies involves a number of practical issues and trade-offs at both architecture and circuit level, that must be taken into account in order to optimize the performance of ΣΔ ADCs in terms of power budget. This problem is aggravated in the case of reconfigurable ADCs intended for SDR systems, since adaptation and reconfiguration features are required in order to cover a tunable region in the resolution-vs-bandwidth plane.
This paper contributes to this topic and presents innovative solutions for the implementation of *flexible* high-efficiency ΣΔ ADCs that can reconfigure their performance to a large number of specifications with scalable power consumption. Novel cascade ΣΔM topologies that combine USTF, loop-filter resonation, as well as the ability to operate concurrently, are analyzed and compared – going from system-level design to practical implementation issues. Measured and simulation results of several case studies – covering a number of standard requirements – are shown to demonstrate the capabilities of the proposed ΣΔMs.

II. Strategies for efficient multi-mode ΣΔMs

Cascade ΣΔMs are more suitable than single-loop architectures for the implementation of reconfigurable ADCs. The modular nature of cascade topologies allows to easily turn different stages on or off depending on the loop-filter order, L, required for a given set of specifications, while keeping system stability and low sensitivity to circuit non-idealities.

A. Reconfiguration and concurrency

Figure 1 shows the conceptual block diagram of a N-stage cascade ΣΔM. All stages can be made independently switchable according to the desired quantization noise shaping, and the Digital Cancellation Logic (DCL), can be

programmed according to the value of L. If a stage is turned off, its building blocks can be powered down to save power. The number of bits of the internal quantizers, B_i, and/or the OverSampling Ratio (OSR) can be also reconfigured in order to increase the *flexibility* of the modulator.

In addition to reconfigure its performance parameters, a multi-mode ΣΔ ADC must digitize signals corresponding to different standards – for instance GSM and Bluetooth signals, and/or UMTS and WLAN signals – in a parallel or *concurrent* way. *Concurrency* can be easily implemented in a cascade ΣΔM as illustrated in Figure 1, where a *concurrent* switch network is used to allow the modulator to be configured as several *sub-modulators* working in parallel – each one processing a different input signal. A number of control signals are needed to enable the switches that correspond to the desired operation mode in each case, either concurrent or cascaded. The DCL processing depends on the concurrent configuration as well as on the number of stages working as either single-loop ΣΔMs or as parts of a cascade [5].

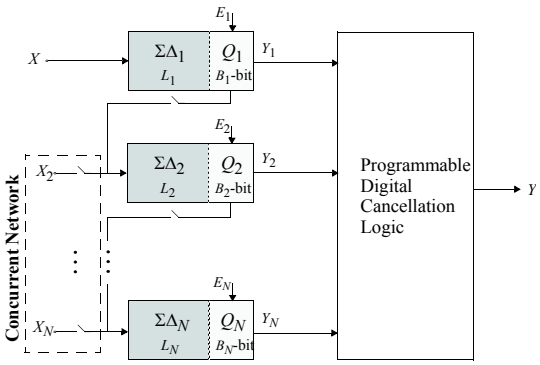


Figure 1. Reconfigurable concurrent ΣΔM.

B. Expandable cascade ΣΔMs with unity STF

The performance of reconfigurable cascade ΣΔMs can be notably improved if USTF is implemented in all stages of the cascade as illustrated in Figure 2. The concept of USTF is based on adding an extra feed-forward path from the input node to the quantizer input (of each stage), so that the integrators ideally process quantization error only and hence, their output swings can be reduced [3].

Assuming a linearized model for the quantizers, the Noise Transfer Function (NTF) of Figure 2 is given by:

$$\mathrm{NTF}(z) = \frac{(1-z^{-1})^L}{d_N} \qquad (1)$$

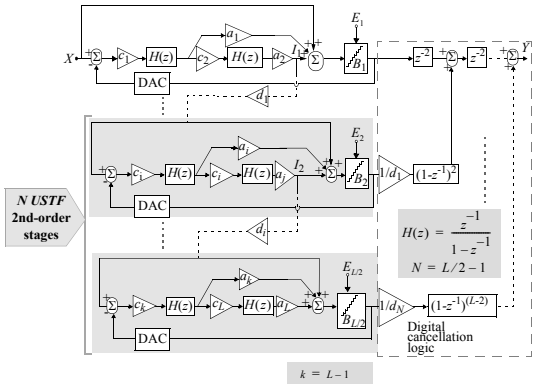


Figure 2. Expandable USTF-based cascade ΣΔM.

As an illustration, Figure 3 shows the measured output spectra of a reconfigurable cascade 2-2 ΣΔM with USTF and 3-level quantization in each stage[1] [2]. Note that the noise-shaping order is adapted to be either L=2 or L=4, according to the signal bandwidth corresponding to each standard, namely: GSM, GPS, UMTS and WiMAX.

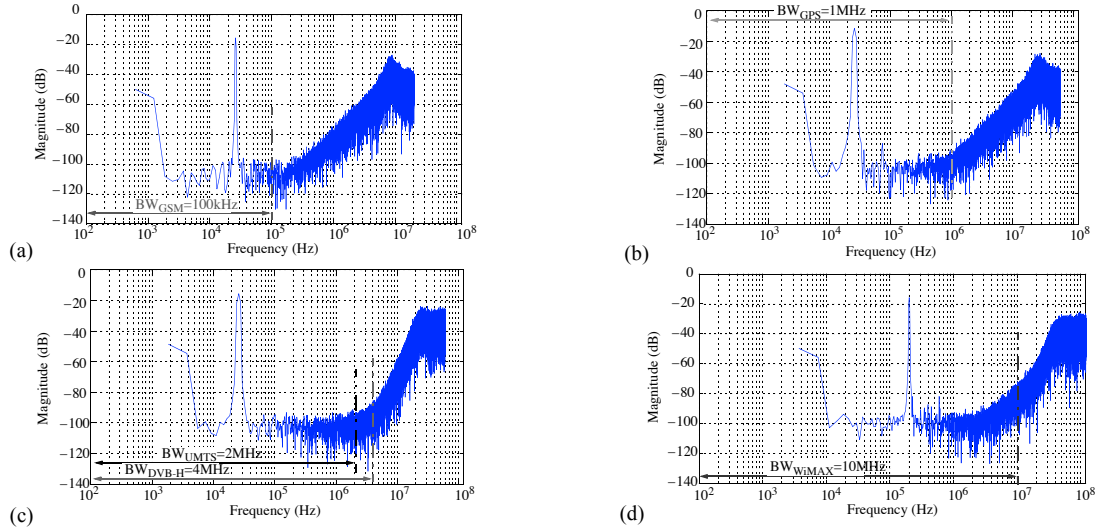


Figure 3. Measured output spectra of a reconfigurable USTF-based cascade 2-2 ΣΔM for different standards: (a) GSM, (b) GPS, (c) UMTS, (d) WiMAX

[1] Details on the chip implementation will be given at the conference.

C. Inter-stage resonation

One way to increase the noise-shaping efficiency of cascade ΣΔMs without penalizing the number of stages – conditioned by noise leakage due to mismatch – consists of including *resonators* in the loop filter. This way, the zeros of NTF are shifted from DC to optimal frequencies that maximize the effective resolution – without increasing the loop filter order, with the subsequent saving in power consumption.
Resonation is usually implemented in the last stage of a cascade in order to keep the same DCL filter as in a *conventional* cascade architecture [6]. Alternatively, an inter-stage resonation loop can be implemented in a 2-stage cascade topology by feeding a scaled version of the back-end quantization error back to the input of the front-end quantizer [7]. Figure 4(a) shows a cascade 2-2 ΣΔM with inter-stage resonation and USTF in both stages which, in contrast to [7], uses only Forward-Euler (FE) integrators, thus simplifying the Switched-Capacitor (SC) implementation and reducing the sensitivity to circuit errors. One of the advantages of using USTF is the reduction of the opamps Output Swing (OS). In the case of Figure 4(a), the required OS is only ±0.15V for the 1st- and the 3rd- opamp, whereas it drops to ±0.10V for the 2nd- and the 4th- opamps.
Assuming a linearized model for the quantizers, it can be shown that the NTF(z) is given by:

$$\mathrm{NTF}(z) = \frac{-(1-z^{-1})^2[1-(2-g)z^{-1}+z^{-2}]}{d_N} \tag{2}$$

Figure 4(b) shows the simulated output spectrum. The action of resonation allows to increase the effective resolution, with no appreciable degradation due to capacitor mismatch. This is illustrated in Figure 4(c), that shows the Effective Number Of Bits (ENOB) for a –6dBFS input signal obtained for a 50-run Monte Carlo simulation considering a standard deviation of 0.1%. The average [m (bits)] and standard deviation, σ, of the ENOB is shown for different standards. In all cases, 4-bit internal quantizers, kT/C noise and a 1-V reference voltage were considered in the simulations.

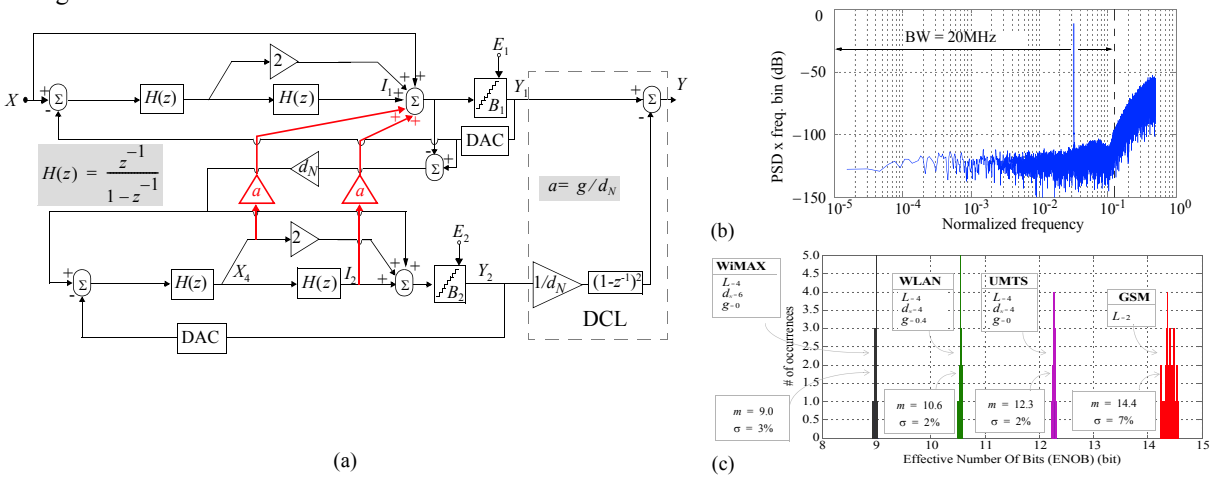


Figure 4. Cascade 2-2 ΣΔM with inter-stage resonation: (a) Block diagram. (b) Output spectrum. (c) Monte Carlo simulation with 0.1% mismatch.

D. Sturdy MASH ΣΔM with USTF

An alternative to *conventional* cascade ΣΔMs that reduces sensitivity to noise leakages is the so-called SMASH ΣΔM. These ΣΔMs replace the DCL by a direct digital subtraction of the stages outputs, with the subsequent elimination of matching requirements between analog and digital filtering [4]. The performance of SMASH ΣΔMs can be improved by using USTF in all stages of the modulator, as illustrated in Figure 5. However, feeding the output of that digital summation back to the modulator input requires a Digital-to-Analog Converter (DAC) with double full scale and one more bit than the largest of the resolutions of the ADCs in the cascade. This could be an important restriction that – depending on the value of B_i – may complicate the circuit implementation.

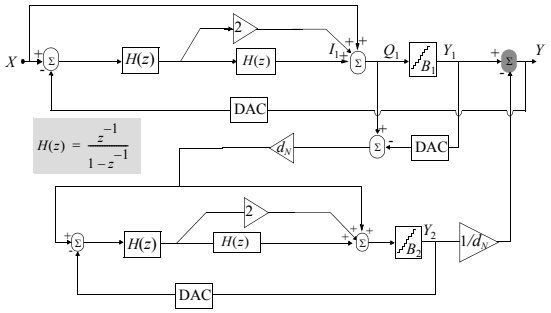


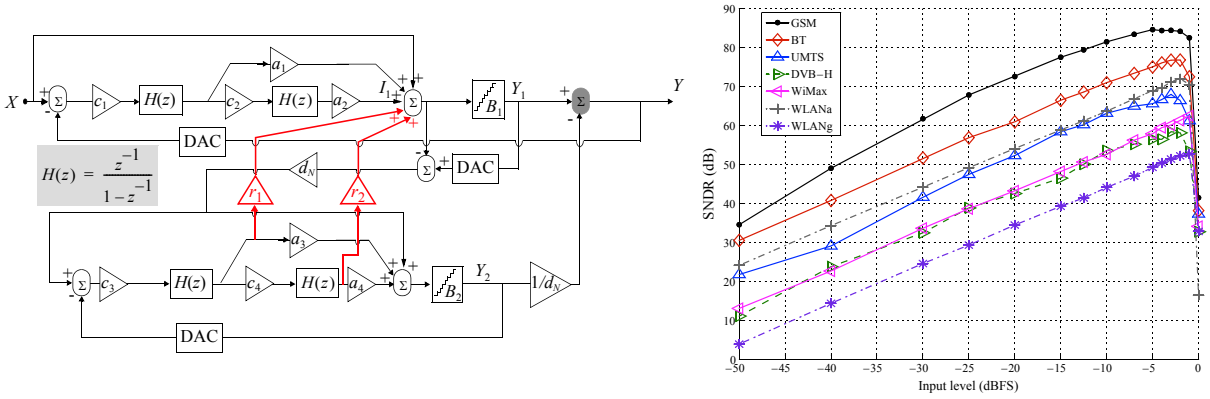
Figure 5. Cascade 2-2 USTF-based SMASH ΣΔM.

III. Putting all pieces together

The strategies described above can be put together in order to improve the efficiency of reconfigurable cascade ΣΔMs. This is illustrated in Figure 6(a), that shows a cascade 2-2 SMASH ΣΔM including inter-stage resonation, multi-bit quantization and USTF in both stages. The NTF of this modulator is given by (2). Global resonation is implemented by two inter-stage paths with gains $r_1 = g/(d_N \cdot c_3)$ and $r_2 = (g \cdot a_4)/d_N$, that feed a delayed version of the last-stage quantization error back to the first-stage quantizer. Note that the modulator in Figure 6(a) uses only FE integrators, thus simplifying the SC implementation and reducing the sensitivity to some circuit errors.

A. Beyond-3G case study

In order to illustrate the suitability of the ΣΔM in Figure 6(a) for multi-standard applications, this modulator was designed for the specifications of seven standards, namely: GSM, Bluetooth (BT), UMTS, DVB-H, WiMAX and WLAN (IEEE 802.11a/n). Considering a direct-conversion radio receiver, it can be shown that the signals of these standards must be digitized with a Signal-to-(Noise+Distortion) Ratio (SNDR) of 80/75/65/55/60/65/50 dB, within BW=0.2/0.5/1.96/3.8/10/10/10/20MHz. These specifications can be achieved with OSR=200/80/40/20/12/16/8; L=2 for GSM, BT, UMTS and DVB-H; and L=4 for WiMAX and WLAN; and a resolution of the first- and the second-stage quantizers of 3 and 5 levels, respectively. Inter-stage resonation is used only in WLAN (IEEE 802.11n mode) with a feedback coefficient of g/d_N=0.05. This reduces the In-Band Error (IBE) power by approximately 9.5dB within a 20-MHz signal bandwidth.
Figure 6(b) shows the simulated SNDR curves for all the operation modes, including the impact of main circuit non-idealities. Note that the ΣΔM overloads close to the Full-Scale (FS) reference voltage in all cases. These results confirm the suitability of this case study for the implementation of ADCs in multi-standard wireless transceivers – a direct consequence of the combined use of USTF, inter-stage resonation and SMASH strategies.



(a) (b)

Figure 6. SMASH ΣΔM with USTF and inter-stage-resonation: (a) Block diagram. (b) SNDR vs. input level.

B. Practical timing issues

The ΣΔMs described in previous sections are cascade architectures based on using USTF in all stages. These kinds of architectures suffer from timing issues in practice what make their circuit implementation very difficult and prone to structural errors. In order to analyse potential timing issues in USTF-based cascade ΣΔMs, let us consider the cascade 2-2 ΣΔM shown in Figure 7. The critical *timing path* is highlighted with symbol ⊗ in the figure. Note that the quantization error of the front-end quantizer, $E_1(z)$, is extracted as a subtraction of two paths (performed in the virtual adder AA_2); namely, one path from Q_1 and another path after the quantization and the inter-stage DAC (labelled as DAC$_i$).

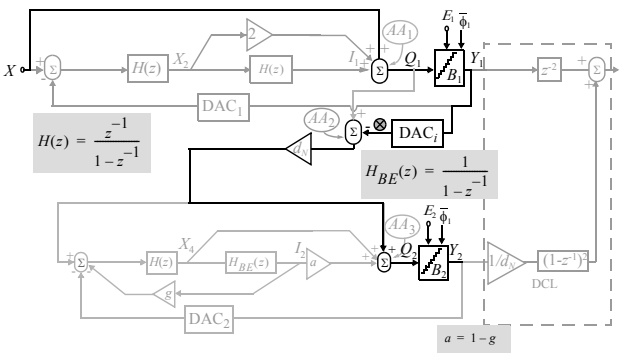


Figure 7. Critical path due to timing issues in USTF-based cascade ΣΔMs.

Practical timing problems arise when $E_1(z)$ is given to the second-stage adder (AA_3) and to the subsequent quantizer (Q_2). This is better illustrated in Figure 8, where the timing problem is depicted in more detail. Figure 8(a) shows the modulator parts where the problem takes place and Figure 8(b) depicts the corresponding timing diagram. The analog adders AA_1 and AA_3 operate in one clock phase, ϕ_1, the embedded quantizers compare their inputs at the end of this phase and the in-loop DAC operates in the following clock phase, ϕ_2. The main issue is given by the fact that DAC_i is activated at ϕ_2. As a result, there is an extra full period delay (z^{-1}) at this point, which avoids the correct extraction of $E_1(z)$. This extra delay may result in practice in a severe degradation in the noise-shaping behavior of the modulator.

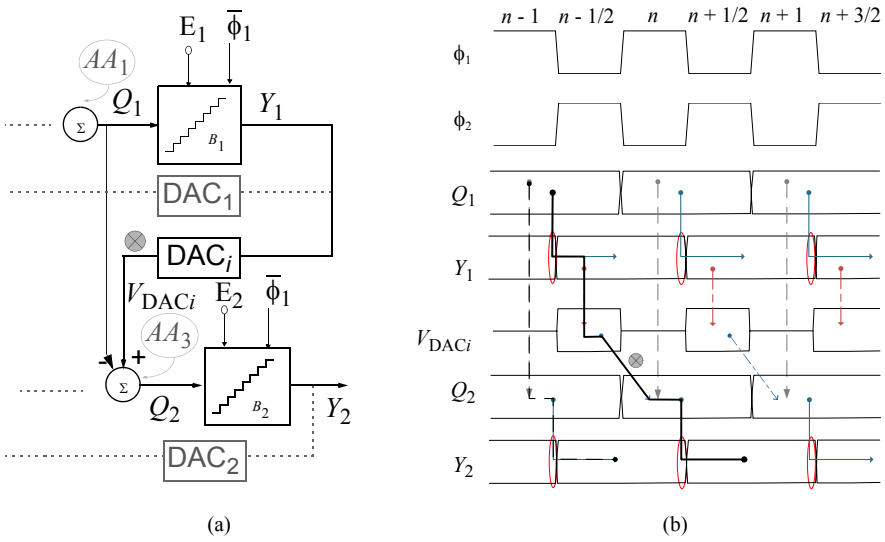


Figure 8. Detailed view of the critical path in Figure 7: (a) Block diagram. (b) Timing scheme.

IV. Proposed SMASH ΣΔM with local and inter-stage resonation

As discussed above, USTF-based cascade ΣΔMs cannot be implemented in practice by extracting the front-end stage quantization error through two inter-stage paths due to timing issues. This problem can be eliminated if only one inter-stage path is used as originally proposed in [3]. Based on this idea, Figure 9 shows the proposed SMASH ΣΔM, that uses USTF only in the front-end stage and combines two types of resonation: inter-stage resonation and local resonation in the front-end stage. In practice, an extra delay is required to correctly extract the quantization error of the back-end stage. To this purpose, the inter-stage global resonator path marked with ⊗ needs to incorporate a full-period delay (z^{-1}). This additional delay can be implemented by three sampled-and-hold SC branches as proposed in [8].

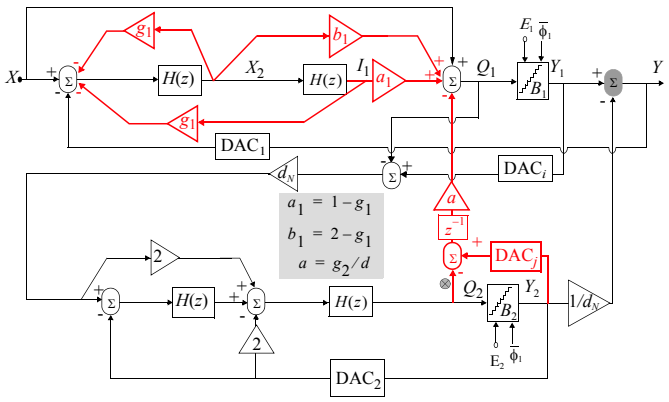


Figure 9. Proposed SMASH ΣΔM with local and inter-stage resonation.

Assuming a linear model for the quantizers in Figure 9(a), it can be shown that the Z-transform of the output is given by:

$$Y(z) = X(z) + [1-(2-g_1)z^{-1}+z^{-2}](1-z^{-1})^2 E_1(z) - \frac{1}{d_N}[1-(2-g_1)z^{-1}+z^{-2}][1-(2-g_2)z^{-1}+z^{-2}]E_2(z) \quad (3)$$

Given that the second-stage does not implement USTF, there is a (4th-order) filtered component of $E_1(z)$ in the modulator output. This is the price to pay in this architecture in order to benefit from the combination of USTF,

resonation and SMASH strategies without timing issues. As an illustration, Figure 10 shows the output spectrum of Figure 9 considering OSR=4, where the effect of both local and inter-stage resonation is illustrated separately.

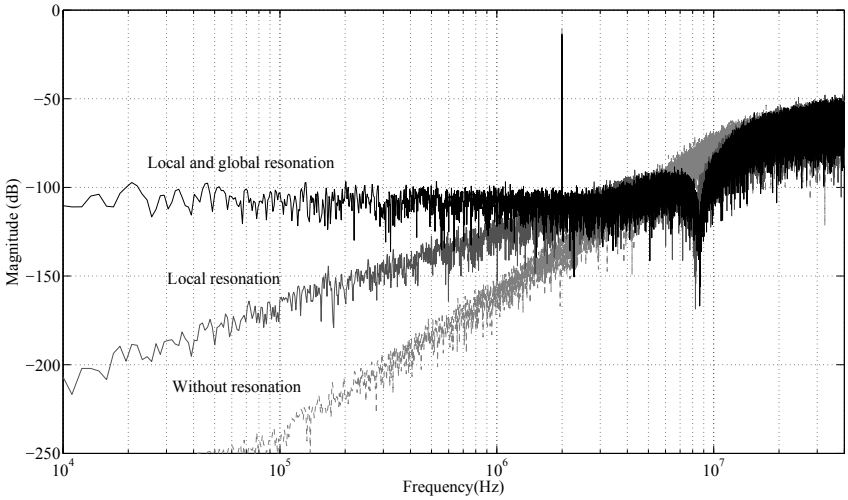


Figure 10. Output spectrum of Figure 9 with OSR=4.

V. Conclusions

Different strategies to implement efficient multi-mode, multi-standard cascade ΣΔMs have been analyzed and compared. Several case studies, including both simulation and experimental results have been shown to illustrate the architectures under study. It has been demonstrated that the combination of SMASH topologies with resonation and USTF in all stages of the cascade give rise to practical timing issues that can completely degrade the performance of the modulator. To avoid this, a novel SMASH 2-2 ΣΔM topology, that is free of the mentioned timing issues has been proposed. The modulator uses USTF only in the frond-end stage, and combines both local and global resonation in order to adapt the performance to different standard specifications. Details on different circuit implementations and chip measurements will be presented at the conference.

Acknowledgments

This work has been supported by the Spanish Ministry of Science and Innovation (with support from the European Regional Development Fund) under contracts TEC2007-67247-C02-01/MIC and TEC2010-14825/MIC, and the Regional Council of Innovation, Science and Enterprise under contract TIC-2532.

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